clock, the timing of the first clock being independent of the timing of the second clock, means for utilizing the second clock to transfer information without synchronization with the first clock from the means for storing information without transferring other [data] information into said means for storing information whereby the information may be immediately utilized by the second component without need for storage by the second component, said means for utilizing the second clock to transfer information without synchronization with the first clock from said means for storing information comprising means for transferring the information in said means for storing information to the second component under control of the second clock, said means for transferring the information in said means for storing information to the second component under control of the second clock includes means for switching the second clock to the terminals used by the first clock, said means for switching the second clock to the terminals used by the first clock includes a multiplexor, said multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said [buffer] means for storing information to transfer [data] information to said second component.

2. (Amended) A computer system as claimed in claim 1 in which the means for utilizing the clock of the second component to transfer information from [the storage of the first component] the means for storing information in a condition in which it is synchronized for use by the second component comprises means for providing a signal to the second component to indicate that a prescribed amount of information has been stored in the [buffer] means for storing information.

3. (Amended) A computer system as claimed in claim 1, in which the means for switching the second clock to the terminals used by the first clock includes means for signaling the multiplexor that the second component is ready to accept the information in [the buffer] the means for storing information.

4. (Amended) A computer system comprising a plurality of components operated in response to timing of different clocks, means for storing information, means for utilizing the clock of any one of the components to transfer information without synchronization of timing of different clocks between one of the components and the means for storing information, means

for signaling any of the components that information stored in the means for storing is to be transferred to that one of the components as a destination component, means for utilizing the clock of the destination component to transfer information from the means for storing information without synchronization of timing of different clocks in a condition in which the information is synchronized for use by the destination component wherein the means for utilizing the clock of any one of the components always utilizes the clock of the component transferring information into said means for storing information, and wherein the timing of the clock of the component from which the information was transferred is independent of the timing of the clock of the destination component, said means for utilizing the clock of the destination component to transfer information from the means for storing information in a condition in which it is synchronized for use by the destination component includes a multiplexor for transferring signals from [addressed components] the destination component to [the means for storage] the means for storing information, said multiplexor coupled to [a first component] the component transferring information into the means for storing information and [a second component] the destination component, said multiplexor receiving a signal from said [second component] the destination component for furnishing a [second] clock signal from [said second clock] the clock of the destination component to [said buffer] the means for storing information to transfer [data] information to [said second component] the destination component.

5. (Amended) A computer system as claimed in claim 4 in which the means for [signaling] signaling [another of the components] a second destination component that the information stored in the means for storing information is to be transferred to the [other of the components] second destination component comprises means for synchronizing a signal from the means for signalling [any one of the components] with the clock of the second destination component.

6. (Unchanged) A computer system as claimed in claim 4 in which the multiplexor comprises an AND gate, and means for transferring gated clock signals from each of the components as inputs to the AND gate.

7. (Amended) A computer system as claimed in claim 6 in which the means for transferring gated clock signals from each of the components as inputs to the AND gate

comprises a plurality of OR gates, each such OR gate connected to receive a clock and a gating signal for transferring the clock from one of the components.

8. (Unchanged) A computer system comprising:

a first component;

a first clock coupled to said first component, said first component operated in response to timing of said first clock;

a buffer coupled to said first component, said first component always using said first clock to transfer data from said first component to said buffer without synchronizing said transfer of said data to another clock;

a second component coupled to said buffer;

a second clock coupled to said second component, the timing of said first clock being independent of the timing of said second clock, said second component reading said data from said buffer using said second clock without synchronizing said reading to another clock and without transferring other data into said buffer;

a multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

9. (Unchanged) A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component operated in response to timing of said third clock, the timing of said third clock being independent of the timing of said first clock,

wherein said first component uses said first clock to transfer further data from said first component to said buffer without synchronizing said transfer of said further data to another clock, and

wherein said third component transfers said further data from said buffer using said third clock without synchronizing said transfer of said further data to another clock.

10. (Unchanged) A computer system as in claim 8 further comprising:

a third component;

a third clock coupled to said third component, said third component operated in response to timing of said third clock the timing of said third clock being independent of the timing of said second clock,

wherein said second component uses said second clock to transfer further data from said second component to said buffer without synchronizing said transfer of said further data to another clock, and

wherein said third component transfers said further data from said buffer using said third clock without synchronizing said transfer of said further data to another clock.

11. (Unchanged) A computer system as in claim 8 wherein said data may be immediately utilized by said second component without storing said data in said second component.

12. (Unchanged) A computer system as in claim 9 wherein said further data may be immediately utilized by said third component without storing said further data in said third component.

13. (Unchanged) A computer system as in claim 8 wherein the transfer of said data into said buffer is controlled entirely by said first component and said first clock.

14. (Unchanged) A method for transferring data between a plurality of components in a computer system including a first and a second component, said method comprising:

operating said first component using a first clock having a first timing;

operating said second component using a second clock having a second timing independent of said first timing;

transferring an entire packet of data having a plurality of words from said first component to a buffer always using said first clock without synchronizing any of said plurality of words to another clock;

once said entire packet of data is transferred from said first component to said buffer, signaling said second component that said entire packet of data is ready to be transferred to said second component;

transferring said entire packet of data to said second component using said second clock without transferring other data into said buffer;

furnishing a clock signal to said buffer from a multiplexor, said multiplexor coupled to said first component and said second component, said multiplexor receiving a signal from the second component for furnishing a second clock signal from said second clock to said buffer to transfer data to said second component.

15. (Unchanged) A method for transferring data as in claim 14, wherein said computer system comprises a third component and wherein said method further comprises:

operating said third component using a third clock having a third timing independent of said first clock;

transferring a further entire packet of data having a second plurality of words from said first component to said buffer using said first clock without synchronizing any of said second plurality of words to another clock;

once said further packet of data is transferred from said first component to said buffer, signaling said third component that said further entire packet of data is ready to be transferred to said third component;

transferring said further entire packet of data to said third component using said third clock without synchronizing any of said second plurality of words to another clock.

16. (Unchanged) A method as in claim 14 wherein said second component uses said entire packet of data immediately without first storing said entire packet of data in said second component.

17. (Unchanged) A method as in claim 15 wherein said third component uses said further entire packet of data immediately without first storing said further entire packet of data in said third component.

18. (Unchanged) A method as in claim 15 wherein said step of signaling said second component occurs by broadcasting a first signal from said first component to said second and third components, said first signal being synchronized to said second clock, and wherein said step of signaling said third component occurs by broadcasting a second signal from said first component to said second and third components, said second signal being synchronized to said third clock.

19. (Unchanged) A computer system as in claim 8 further comprising:

a bus for carrying a first signal, said bus being coupled to said first component and said second component, said first signal being provided by said first component and being synchronized to said second clock, said first signal being received by said second component and causing said second component to read said data from said buffer.

20. (Unchanged) A computer system as in claim 9 further comprising:

a bus for carrying a first signal and a second signal, said bus being coupled to said first, second and third components, wherein said first signal is provided by said first component and is synchronized to said second clock, said first signal being received by said second component and said third component and causing said second component to read said data from said buffer, and wherein said second signal is provided by said first component and is synchronized to said third clock, said second signal being received by said third component and by said second component and causing said third component to read said further data from said buffer.

21. (Unchanged) A computer system as in claim 19 wherein said data comprises a plurality of words having a selected number of words and wherein said plurality of words are transferred to said buffer without synchronizing any of said plurality of words to any clock except said first clock and wherein said first signal is received by said second component after all of said plurality of words are transferred to said buffer and wherein all of said plurality of words are transferred to said second component from said buffer after said second component receives said first signal.

22. (Unchanged) A computer system as in claim 20 wherein said data comprises a plurality of words having a selected number of words, and wherein said plurality of words are transferred to said buffer without synchronizing any of said plurality of words to any clock except said first clock and wherein said first signal is received by said second component after all of said plurality of words are transferred to said buffer, and wherein all of said plurality of words are transferred to said second component from said buffer after said second component receives said first signal, and wherein said further data comprises a further plurality of words, and wherein said further plurality of words are transferred to said buffer without synchronizing any of said further plurality of words to any clock except said first clock and wherein said second signal is received by said third component after all of said further plurality of words are transferred to said buffer and wherein all of said further plurality of words are transferred to said third component from said buffer after said third component receives said second signal.

23. (New) An apparatus for use in a computer system for transferring data from a first component to a second component, the first component clocked by a first clock signal, and the second component clocked by a second clock signal, the timing of the first clock signal being independent of the timing of the second clock signal, the apparatus comprising:

a buffer coupled to the first component and the second component via a data path, the first component always using the first clock signal to transfer data from the first component to the buffer without synchronizing the transfer of the data to another clock; and

a multiplexer having inputs coupled to the first clock signal and the second clock signal, and an output coupled to the buffer, the multiplexer supplying the first clock signal to the buffer to clock data from the first component to the buffer via the data path in the absence of a valid signal from the second component, and in response to the valid signal from the second component, supplying the second clock signal to the buffer to clock data from the buffer to the second component via the data path without clocking other data from the first component to the buffer via the data path.

24. (New) The apparatus of claim 23, wherein a ready signal from the first component is transmitted to the second component indicating that the transfer of data from the first component to the buffer is complete.

25. (New) The apparatus of claim 23, wherein the buffer and multiplexer are part of an integrated circuit.

26. (New) A method of transferring data between a first component and a second component in a computer system, the first component clocked by a first clock signal, and the second component clocked by a second clock signal, the timing of the first clock signal being independent of the timing of the second clock signal, comprising:

clocking data from the first component to a buffer via a data path using the first clock signal in the absence of a valid signal from the first component, the first component always using the first clock signal to transfer data from the first component to the buffer without synchronizing the transfer of the data to another clock;

clocking data from the buffer to the second component via the data path using the second clock signal in response to the valid signal from the second component without clocking other data from the first component to the buffer via the data path; and

supplying the first and second clock signals to the buffer via a multiplexer having a plurality of inputs and an output coupled to the buffer, the inputs for receiving the first and second clock signals and a valid signal from the second component, the multiplexer supplying the second clock signal to the buffer in response to the valid signal.

27. (New) The method of claim 26, further comprising transmitting a ready signal from the first component to the second component indicating that the transfer of data from the first component to the buffer is complete.

28. (New) An apparatus for use in a computer system for transferring data between a plurality of components including at least one source component and at least one destination

component, the source component clocked by a first clock signal, and the destination component clocked by a second clock signal, the timing of the first clock signal being independent of the timing of the second clock signal, comprising:

a buffer coupled to the source component and the destination component via a data path, the source component always using the first clock signal to transfer data from the source component to the buffer without synchronizing the transfer of the data to another clock;

a multiplexer having inputs coupled to the first clock signal and the second clock signal, and an output coupled to the buffer, the multiplexer supplying the first clock signal to the buffer to clock data from the source component to the buffer via the data path in the absence of a gate signal from the destination component, the multiplexer supplying the second clock signal to the buffer to clock data from the buffer to the destination component via the data path in response to the gate signal from the destination component without clocking other data from the source component to the buffer via the data path; and

a broadcast bus coupled to the source component, the destination component and the buffer, the broadcast bus for transferring a ready signal from the source component to the destination component indicating that the transfer of data from the first component to the buffer is complete.

29. (New) The apparatus of claim 28, wherein the source component places the address of the destination component on the broadcast bus and the destination component supplying the gate signal to the multiplexer in response to the address.

30. (New) The apparatus of claim 28, wherein the buffer and the multiplexer are part of an integrated circuit.

REMARKS

Claims 1-30 are pending and stand rejected. Applicants have amended claims 1-5, 7, 23, 26 and 28.